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TR 921019-1

Technical Report on

"Development of 6H-SiC CMOS Transistors for Insertion into a 350°C Operational Amplifier"

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I. Summary

Wafers with epitaxial layers have been grown for both n-channel and p-channel 6H-SiC MOSFETs. The device fabrication for each of these devices has been initiated and is on-going. Both types of devices will utilize ion implanted source and drain wells and will have molybdenum gate contacts that overlap the implanted wells. The same interdigitated mask design will be used for both of the devices. Eight wafers for p-channel devices are being held until the first batch of these devices is completed.

Device parameter measurements have been made on n-channel MOSFET devices that were fabricated prior to this contract. These parameters will be used to simulate circuits using Simulation Program with Integrated Circuit Emphasis (SPICE). Three approaches have been examined for designing circuits using both NMOS and PMOS transistors in a complementary design. These include a hybrid approach that uses NMOS and PMOS devices fabricated on separate wafers, a shared substrate approach that uses an enhancement-mode PMOS device and a depletion-mode NMOS device, and a traditional single substrate CMOS approach utilizing PMOS and NMOS devices that both operate in *enhancement-mode*.

II. Background

For this Phase I effort, it was proposed to fabricate and characterize both p-channel and n-channel MOSFETs in 6H-SiC. While there has been some development of n-channel MOSFETs in 6H-SiC previous to this effort, they are still in the very early stages of development. To date there have been no p-channel MOSFETs reported in the literature. Therefore, it was proposed to fabricate both types of these devices and then fully characterize them from room temperature to 350°C. This effort would include the development of improved processes for oxide growth and contact annealing for 6H-SiC, as well as the other necessary device fabrication techniques that are required for these devices.

The data obtained for these devices would then be used to model both device parameter optimization and circuit simulation (SPICE) to accurately predict the characteristics that can be expected from a high temperature operational amplifier

to be fabricated and tested during Phase II. The device modeling and circuit simulation that was proposed was to be conducted by Dr. John Paulos, an Associate Professor in the Department of Electrical and Computer Engineering at North Carolina State University (NCSU).

III. MOSFET Device Development

A. n-channel MOSFETs

Seven wafers have been grown for the fabrication of n-channel MOSFETs. The p-type wafers were sawed from Al-doped p-type 6H-SiC single crystal boules. The substrates were then diamond polished on the (0001) Si-face. The carrier concentration of the substrates ranged from $p = 1.3\text{-}3.3\times10^{18}$ cm^{-3}. Epitaxial thin films of Al-doped 6H-SiC were then grown on the substrates, with a thickness of 3 μm and carrier concentrations in the range of $p = 3\text{-}10\times10^{15}$ cm^{-3}.

After the epitaxial layers were grown, the device fabrication was initiated. The device structure is shown in cross-section in Fig. 1. The source and drain wells are to be formed by ion implantation of N^+ at high temperature (650°C), using polysilicon as the implant mask. Because of the high temperature anneal required for dopant activation after the ion implantation step, the wafers must be stripped clean. Therefore alignment marks must first be reactive ion etched into the wafer surface in order to be able to align the patterns to the ion implanted wells after the high temperature anneal. The source and drain ohmic contact metal that will be used is annealed nickel, while the gate contact metal will be molybdenum. The ground contact on the back of the substrate will be titanium. The device pattern, shown in Fig. 2, utilizes an interdigitated pattern, with three source fingers on the left and two drain fingers on the right. The gate contact weaves in between these fingers, overlapping the ion implanted wells (which can not be seen in the micrograph). Four different gate lengths are included on this mask set, being 7 μm, 10 μm, 15 μm, and 20 μm. The gate width for all of these patterns is 1 mm.

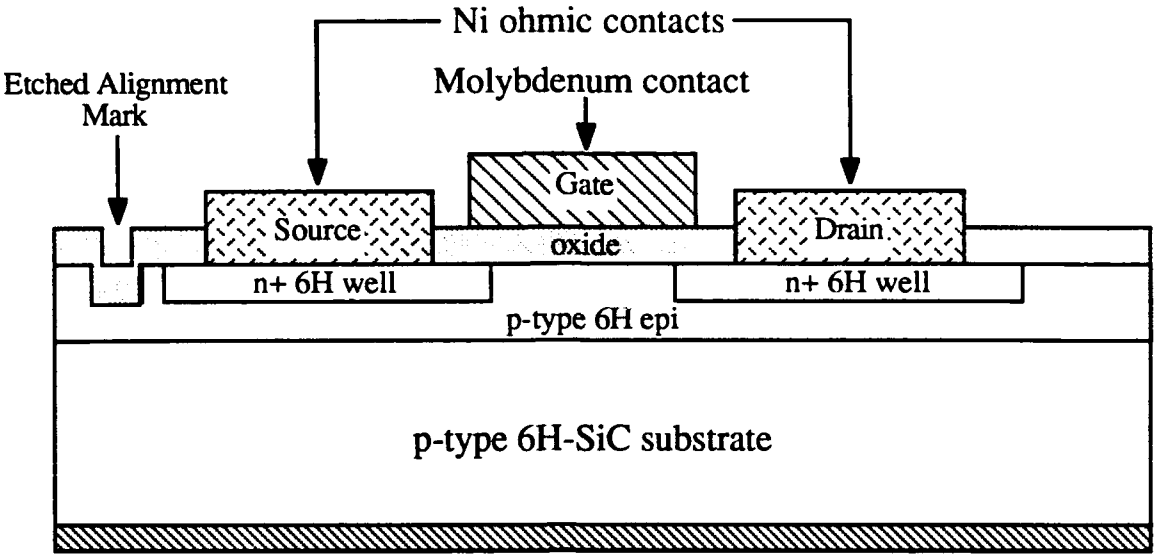


Figure 1: Cross-sectional view of the 6H-SiC n-channel MOSFET design, utilizing ion implanted source and drain wells.

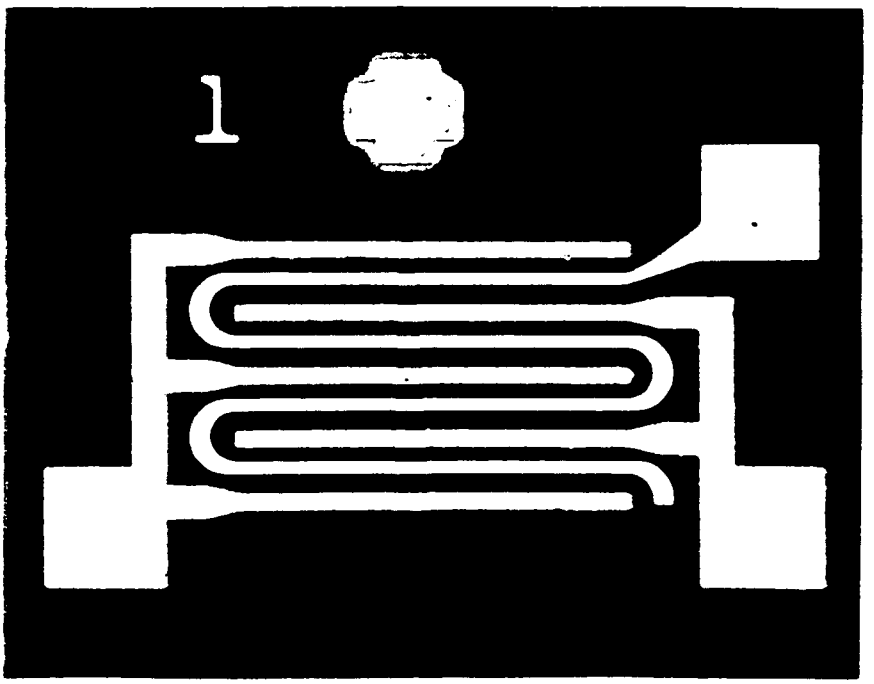


Figure 2: Interdigitated structure of a high temperature 6H-SiC n-channel MOSFET. The source and drain contacts are at the lower left and right, respectively, and the gate contact pad is at the upper right. The gate length and width are 7 μm and 1 mm, respectively.

These wafers are currently in the device processing stage. The implant alignment marks have been reactive ion etched into the wafer surface, and the polysilicon implant mask material has been deposited and patterned. The wafers are now ready for ion implantation. It is anticipated that these devices will be finished by the end of June 1992.

B. p-channel MOSFETs

Sixteen wafers have been grown for the fabrication of p-channel MOSFETs. The n-type wafers were sawed from N-doped n-type 6H-SiC single crystal boules. The substrates were then diamond polished on the (0001) Si-face. The carrier concentration of the substrates ranged from $n = 0.5\text{-}1.6\times10^{18}$ cm^{-3}. Epitaxial thin films of N-doped 6H-SiC were then grown on the substrates, with a thickness of 3 μm and carrier concentrations in the range of $n = 3\text{-}40\times10^{15}$ cm^{-3}. This wide variation in channel doping was used to allow insight into the effect of the channel doping on the I-V characteristics.

As was the case for the n-channel MOSFETs, the device fabrication for eight of the p-channel MOSFETs has been initiated. The other eight wafers will be held until the first batch is completed. The second batch will then be processed with any necessary improvements that are discovered during the fabrication of the first batch. The device structure for these wafers is shown in cross-section in Fig. 3. The source and drain wells are to be formed by ion implantation of Al^+ at high temperature (650°C), again using polysilicon as the implant mask. These implants will also require a high temperature anneal for dopant activation after the ion implantation step. The source and drain ohmic contact metal that will be used is a proprietary aluminum-based alloy, while the gate contact metal will be molybdenum. The ground contact on the back of the wafer will be annealed nickel. The device pattern to be used is the same as was shown in Fig. 2, utilizing the same mask set.

These wafers are at the same stage of device processing as the n-channel devices. The implant alignment marks have been reactive ion etched into the wafer surface, and the polysilicon implant mask material has been deposited and patterned. The wafers are now ready for Al^+ ion implantation. It is anticipated that these devices will also be finished by the end of June 1992.

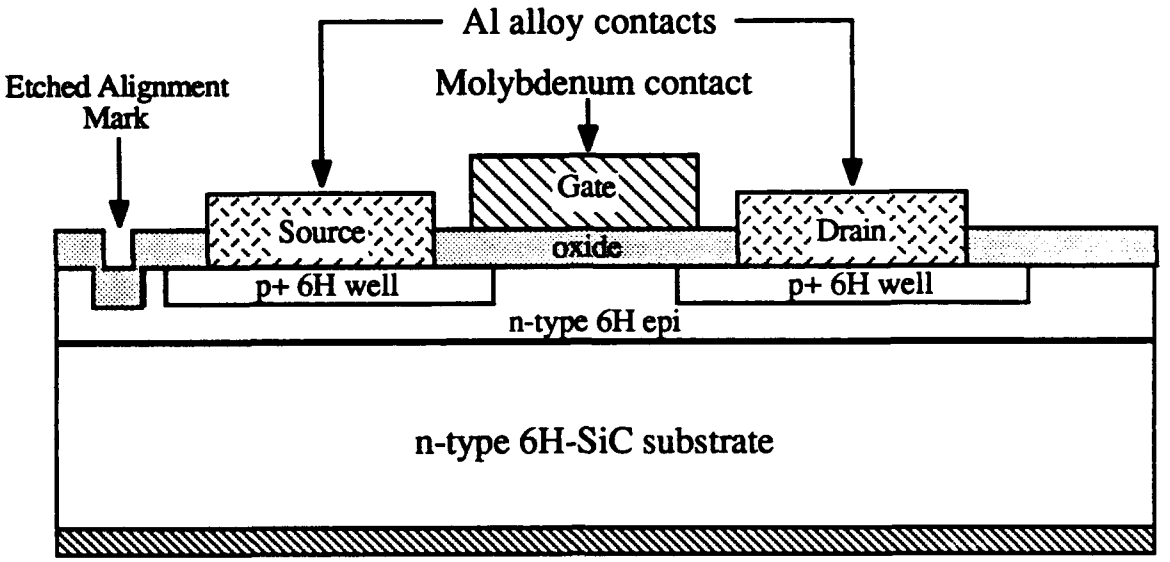


Figure 3: Cross-sectional view of the 6H-SiC p-channel MOSFET design, utilizing ion implanted source and drain wells.

IV. Initial Modeling for 6H-SiC CMOS Operational Amplifier

A feasibility study has been performed in conjunction with Dr. John J. Paulos and his graduate student Tricia Eckman, both of North Carolina State University, to investigate possible ways to design circuits using both NMOS and PMOS transistors (complementary process) in silicon carbide. Three approaches have been examined. The first is a hybrid approach in which NMOS and PMOS transistors are fabricated on separate wafers. These wafers would be sliced into individual die and packaged together using bond wires to interconnect the NMOS and PMOS devices. This approach is the simplest of the three in terms of transistor process development, however, the circuit performance will be adversely affected by the parasitic capacitances associated with the bond wires.

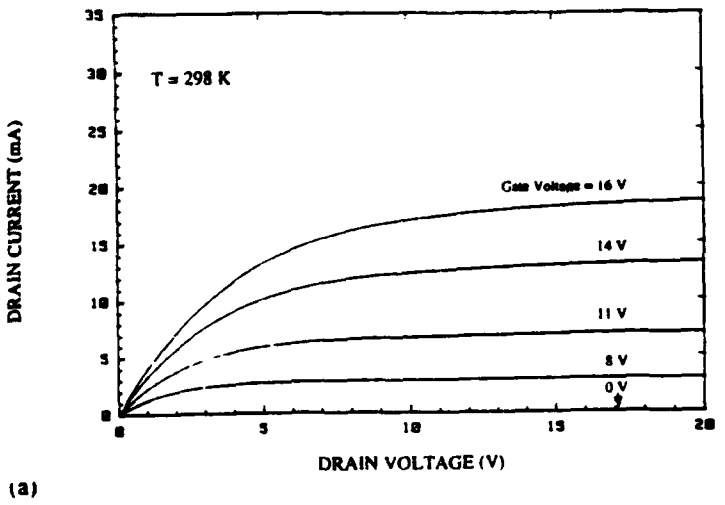
A second approach would utilize a shared substrate in which both NMOS and PMOS transistors are fabricated on a p-type wafer with an n-type epitaxial layer. Isolation would be achieved by etching around the transistor active areas, leaving each transistor in its own mesa. With this approach, the PMOS transistor is a true enhancement-mode MOSFET and the NMOS transistor (fabricated in n-type material)

acts as a depletion-mode device and can be modeled as a MOSFET in parallel with a body resistor. Selective etching of the mesa structure would allow the NMOS transistor epitaxial thickness to be more shallow than the PMOS transistor epitaxial thickness in order to reduce the off-resistance associated with the NMOS device while maintaining breakdown reliability of the PMOS device. This approach appears to be the least favorable due to the added complexity of selective etching and the poor performance of the NMOS transistor.

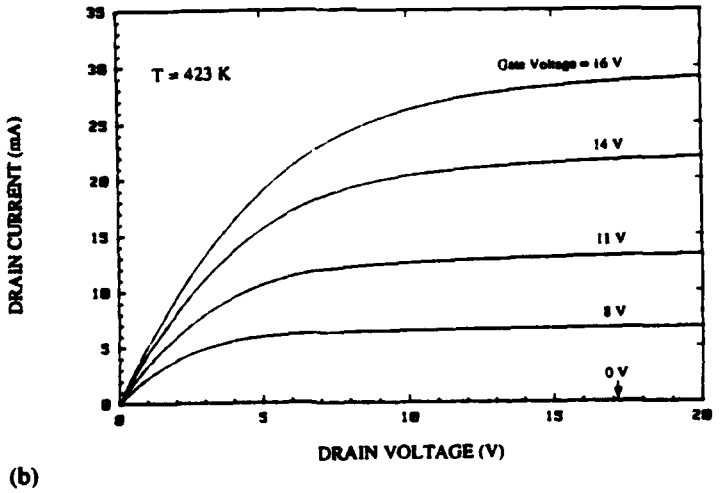
The last approach studied is a true complementary process using multiple epitaxial layers to provide each transistor with the appropriate substrate material. A p-type epitaxial layer would be grown on a p-type substrate for fabrication of the NMOS transistor. An n-type epitaxial layer would then be grown on the p-type epitaxial layer for fabrication of the PMOS transistors. The n-type layer would be etched to form mesas for the PMOS transistor. An extra contact for each layer has to be provided in order to properly bias each "substrate". This approach is the most promising from a circuit performance standpoint as both the NMOS and the PMOS devices are true enhancement-mode MOSFETs.

In order to properly simulate circuits using SPICE (Simulation Program with Integrated Circuit Emphasis), models must be developed that reflect the characteristics of the devices to be used. Individual NMOS transistors which had been fabricated previous to this contract are currently being tested at room temperature and at elevated temperature (up to 350°C) to determine their operating characteristics. Typical I-V curves for the n-channel devices that are being measured are shown as a function of temperature in Fig. 4. A variety of parameters are being recorded, including threshold voltage, transconductance, output resistance, and effect of substrate bias. Parameter optimization will be performed to obtain SPICE level 3 parameters which provide good fit to the experimental data.

As the new devices being fabricated under this effort become available, these measurements will be repeated. Of particular interest will be the characterization of the p-channel devices, since none have been successfully fabricated to date and their is no reported characteristics for these devices. Therefore, finishing the device fabrication of the p-channel devices as early as possible is considered a priority for this program.



(a)



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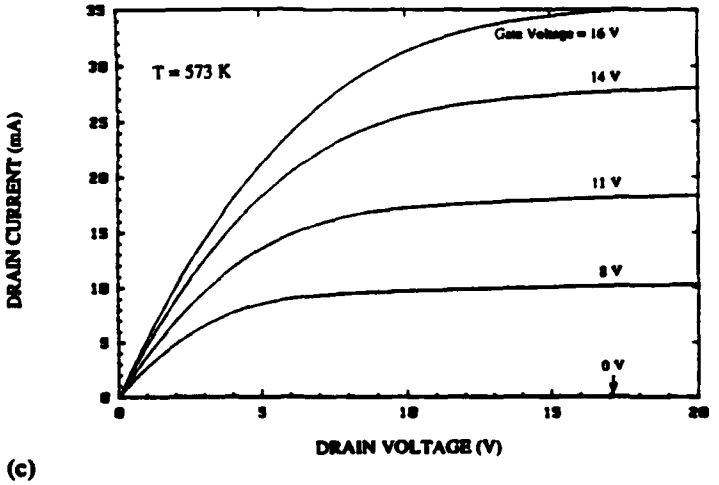

(c)

Figure 4: Drain current-voltage characteristics of an n-channel 6H-SiC enhancement-mode MOSFET at (a) 25°C, (b) 150°C, and (c) 300°C. The gate length and width were 7 μm and 1000 μm, respectively.

SPICE will be used to design an operational amplifier (opamp) using the models developed for the silicon carbide transistors. Two of the three process approaches proposed above will be used to show two possible opamp designs. A hybrid opamp will be designed using the silicon carbide device models and incorporating parasitic capacitances associated with hybrid packaging, and a true complementary opamp will be designed using the same silicon carbide device models and incorporating small on-chip parasitic capacitances.

Circuit performance will be assessed to determine the impact of the hybrid parasitics and to identify possible changes in processing to improve device performance. Feedback will be provided during transistor testing and circuit design to the experimental portion of the project.

V. Plans for Next Period

Fabrication of the n-channel and p-channel MOSFETs discussed in Section III will be continued and finished during the next two months. These devices will then be fully characterized so the device parameters can be included in the SPICE modeling effort. Additionally, if the p-channel MOSFET wafers are unsuccessful, or if methods of improvement for these device are obvious, a second batch of p-channel MOSFETs will be fabricated.

The modeling efforts will continue to try and fit curves for n-channel devices to the experimental data that has been obtained. When data is available from the p-channel devices, the modeling for the opamp will be developed.